UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,683	05/11/2001	Kaoru Adachi	0905-0259P-SP	4835

2292 7590 03/18/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,683	ADACHI, KAORU	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 18th of February 2004. Claims 1, 3 and 6 have been amended; claim 5 has been canceled; and no claim has been newly added since the last Office Action was mailed on 18th of November 2003. Currently, claims 1-4 and 6 are pending in this application.

Claim Objections

2. Claims 3 and 4 are objected to because of the following informalities:

In the claim 3, it recites the subject matter "a control circuit" in lines 5-6, and the limitation "said control circuit controls said switch circuit so as to turn on the bus connection" in lines 8-10. However, the parent claim 1 already limits the subject matter "a control circuit" in line 10 with the limitation "said control circuit for controlling said switch circuit so as to turn on the bus connection" in lines 10-13. In fact, the subject matter "a control circuit" in the claim 3 should be the same subject matter that the subject matter "a control circuit" in the parent claim 1 in light of the specification. Therefore, the term "a control circuit" in the claim 3 could be considered as --said control circuit-- because of the above mentioned reason. The claim 4 is a dependent claim of the claim 3.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim 4 recites the limitation "said output circuit" in line 3. There is insufficient antecedent basis for this limitation in the claim. Therefore, the term "said output circuit" could be considered as --an output circuit-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. [JP 2000020459 A; hereinafter Nakajima] in view of Kelley et al. [US 6,134,621 A; hereinafter Kelley] and what was well known in the art, as exemplified by Higaki et al. [US 5,481,679 A; hereinafter Higaki].

Referring to claim 1, Nakajima discloses an electronic instrument (Fig. 1) in which a device for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1), a device for low-speed access (e.g., LAP-B 3b of Usual Access Field 3 in Fig. 1) and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling transfer of data to these devices (See Solution in Abstract) are connected by a common bus (i.e., data bus 4 of Fig. 1) in such a manner that transfer of data to said device for high-speed access (i.e., SRAM 2b of Fig. 1) takes priority (See col. 5, lines 16-20 and col. 6, line 39 through col. 7, line 1; i.e., wherein in fact that if the access instructions to which access operation to the rapid access field from the CPU is urged are detected, it constitutes from the bus control section which carries out change control of the bus switch so that the data bus between the usual access field may usually be carried out to the CPU at OFF implies that said common bus operates in such a manner that transfer of data to said device for high-speed access takes priority), said electronic instrument comprising: a switch circuit (i.e., bus switch 5 of Fig. 1) for performing control to turn on and off (i.e., ON/OFF) said bus connection between said device for high-speed access and said device for low-speed access (See col. 6, line 39 through col. 7, line 32); and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling said switch circuit so as to turn off said bus connection when data is transferred to said device for high-speed access (See col. 6, line 47 through col. 7, line 1) and turn on said bus connection when data is transferred to said device for low-speed access (See col. 6, lines 39-47).

Nakajima does not expressly teach said device for high-speed access, said device for low-speed access and said switch control circuit each operates in synchronization with common clock pulses, said common clock pulses having a period that varies based on said access speed of said device to be accessed.

Kelley discloses a variable slot configuration for multi-speed bus (See Abstract), wherein a device for high-speed access (i.e., 66 MHz card), a device for low-speed access (i.e., 33 MHz card) and a switch control circuit (i.e., frequency control logic 121 of Fig. 1) each operates in synchronization with common clock pulses (i.e., clock 112 from clock control 66/33 MHz 111 in Fig. 1; See col. 2, lines 15-21), said common clock pulses having a period that varies (i.e., clock periods for 33 MHz or 66MHz) based on said access speed of said device to be accessed (i.e., based on access 66MHz card or 33 MHz card; See Fig. 3).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said common clock pulses control, as disclosed by Kelly, in said electronic instrument, as disclosed by Nakajima, for the advantage of providing mechanism to drive said high-speed access device and said low-speed access device (i.e., 33 MHz card and 66 MHz card) in synchronization with said low-speed clock pulses (i.e., 33 MHz; See Kelly, col. 1, lines 22-41).

Nakajima, as modified by Kelly, does not expressly teach said electronic instrument is implemented in an integrated circuit.

The Examiner takes Official Notice that said electronic instrument being implemented in an integrated circuit, is well known to one of ordinary skill in the art, as evidenced by Higaki (See Fig. 3 and col. 1, lines 15-21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said electronic instrument, as disclosed by Nakajima, as modified by Kelly, in an integrated circuit since it would have been prevalent (See Higaki, col. 1, lines 15-17) for the advantage of reducing a mass-manufacturing cost, minimizing a consuming power requirement, and achieving a small size and a light weight.

Referring to claim 6, Nakajima discloses a method of controlling an electronic instrument (Fig. 1 and See Abstract) in which a device for high-speed access (e.g., SRAM 2b of Rapid Access Field 2 in Fig. 1), a device for low-speed access (e.g., LAP-B 3b of Usual Access Field 3 in Fig. 1) and a control circuit (i.e., bus control section 6 of Fig. 1) for controlling transfer of data to these devices (See Solution in Abstract) are connected by a common bus (i.e., data bus 4 of Fig. 1) in such a manner that transfer of data to said device for high-speed access (i.e., SRAM 2b of Fig. 1) takes priority (See col. 5, lines 16-20 and col. 6, line 39 through col. 7, line 1; i.e., wherein in fact that if the access instructions to which access operation to the rapid access field from the CPU is urged are detected, it constitutes from the bus control section which carries out change control of the bus switch so that the data bus between the usual access field may usually be carried out to the CPU at OFF implies that said common bus operates in such a manner that transfer of data to said device for high-speed access takes priority), said method comprising: providing a switch circuit (i.e., bus switch 5 of Fig. 1) for performing control to turn on and off (i.e., ON/OFF) said bus connection between said device for high-speed access and said device for low-speed access (See col. 6, line 39 through col. 7, line 32); and controlling said switch circuit so as to turn off said bus connection when data is transferred to said device for high-speed access (See col. 6, line 47 through col. 7, line 1) and turn on said bus connection when data is transferred to said device for low-speed access (See col. 6, lines 39-47).

Nakajima does not expressly teach operating said device for high-speed access, said device for low-speed access and said switch control circuit in synchronization with common clock pulses, said common clock pulses having a period that varies based on said access speed of said device to be accessed.

Kelley discloses a variable slot configuration for multi-speed bus (See Abstract), wherein operating a device for high-speed access (i.e., 66 MHz card), a device for low-speed access (i.e., 33 MHz card) and a switch control circuit (i.e., frequency control logic 121 of Fig. 1) in synchronization with common clock pulses (i.e., clock 112 from clock control 66/33 MHz 111 in Fig. 1; See col. 2, lines 15-21), said common

clock pulses having a period that varies (i.e., clock periods for 33 MHz or 66MHz) based on said access speed of said device to be accessed (i.e., based on access 66MHz card or 33 MHz card; See Fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said common clock pulses control, as disclosed by Kelly, in said electronic instrument, as disclosed by Nakajima, for the advantage of providing mechanism to drive said high-speed access device and said low-speed access device (i.e., 33 MHz card and 66 MHz card) in synchronization with said low-speed clock pulses (i.e., 33 MHz; See Kelly, col. 1, lines 22-41).

Nakajima, as modified by Kelly, does not expressly teach said electronic instrument is implemented in an integrated circuit.

The Examiner takes Official Notice that said electronic instrument being implemented in an integrated circuit, is well known to one of ordinary skill in the art, as evidenced by Higaki (See Fig. 3 and col. 1, lines 15-21).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said electronic instrument, as disclosed by Nakajima, as modified by Kelly, in an integrated circuit since it would have been prevalent (See Higaki, col. 1, lines 15-17) for the advantage of reducing a mass-manufacturing cost, minimizing a consuming power requirement, and achieving a small size and a light weight.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima [JP 2000020459 A] and Kelley [US 6,134,621 A] as applied to claims 1 and 6 above, and further in view of Cepulis et al. [US 6,061,754 A; hereinafter Cepulis].

Referring to claim 2, Nakajima, as modified by Kelly, discloses all the limitations of the claim 2 including a plurality of devices (i.e., FROM 2a, SRAM 2b, I/O 3a and LAP-B 3b in Fig. 1; Nakajima) inclusive of said device for high-speed access (i.e., SRAM 2b of Rapid Access Field 2 in Fig. 1; Nakajima) and said device for low-speed access (i.e., LAP-B 3b of Usual Access Field 3 in Fig. 1;

Nakajima) are connected by said common bus (i.e., data bus 4 of Fig. 1; Nakajima) so as to be given priority for data transfer in order of decreasing access speed (See Nakajima, col. 7, lines 46-49; in fact, higher priority is given to a device in Rapid Access Field, e.g., SRAM 2b, by the bus switch and by the neighborhood of CPU); said switch circuit (i.e., bus switch 5 in Fig. 1; Nakajima) being provided between mutually adjacent devices (i.e., between SRAM of Rapid Access Field and LAP-B of Usual Access Field; Nakajima) among said plurality of devices for turning on and off (i.e., connecting and cutting; Nakajima) said bus connection between said mutually adjacent devices among said plurality of devices (See Nakajima, col. 6, line 39 through col. 7, line 32), except that does not expressly teach said control circuit controlling said switch circuits in sequence to turn on said bus connection so as to make possible access to a device circuit having a higher access speed.

Cepulis discloses a data bus having switch for selectively connecting and disconnecting devices to or from the bus (See Abstract and Fig. 8), wherein a plurality of devices (i.e., Bus Agents 841-846 in Fig. 8) inclusive of a device for high-speed access (e.g., Bus Agent 842 in Fig. 8) and a device for low-speed access (e.g., Bus Agent 843 in Fig. 8) are connected by a common bus (i.e., bus 810 of Fig. 8) so as to be given priority for data transfer in order of decreasing access speed (See col. 7, line 66 through col. 8, line 31) among said plurality of devices for turning on and off (i.e., close and open) a bus connection between said mutually adjacent devices among said plurality of devices (i.e., closing/opening bus connections at bus switch 851, at bus switch 852, at bus switch 853 and at bus switch 854, See col. 6, line 39 through col. 7, line 32); a control circuit (i.e., means for controlling the state of the bus switch; See col. 2, line 57) controlling said switch circuits in sequence to turn on said bus connection so as to make possible access to a device circuit (i.e., Bus Agent) having a higher access speed (See col. 2, lines 42-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have expanded the function of said control circuit (i.e., bus control section 6 of Fig. 1) for controlling said switch circuit, as disclosed by Nakajima, as modified by Kelly, to the function of said

control circuit (i.e., means for controlling the state of the bus switch) for controlling said switch circuits (i.e., plural bus switches), as disclosed by Cepulis, for advantage of providing an ability to maximize data transfer rates on the bus (See Cepulis, col. 3, lines 16-18).

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima [JP 2000020459 A] and Kelley [US 6,134,621 A] as applied to claims 1 and 6 above, and further in view of Tsukamoto [US 3,594,656].

Referring to claim 3, Nakajima, as modified by Kelly, discloses all the limitations of the claim 3 including said control circuit (i.e., bus control section 8 of Fig. 1; Nakajima) controls said switch circuit (i.e., bus switch 5 of Fig. 1; Nakajima) so as to turn on said bus connection (See Fig. 1; Nakajima), except that does not expressly teach said control circuit for outputting, in sync with said common clock pulses, a data-transfer enable signal that enables transfer of data upon elapse of a fixed period of time after said control circuit controls said switch circuit so as to turn on said bus connection.

Tsukamoto discloses an automatic clock frequency-switching system (See Fig. 1 and Abstract), wherein a control circuit (i.e., clock frequency control 16 of Fig. 1) for outputting, in sync with common clock pulses (i.e., clock signal), a data-transfer enable signal (i.e., frequency-switching signal via line 19c in Fig. 1) that enables transfer of data (See col. 2, lines 68-72) upon elapse of a fixed period of time (i.e., predetermined time has been elapsed; See col. 4, lines 43-51) after said control circuit controls a switch circuit (i.e., frequency selector 12 of Fig. 1; See col. 2, lines 63-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said automatic clock frequency-switching system, as disclosed by Tsukamoto, in said integrated circuit, as disclosed by Nakajima, as modified by Kelly, so as said changed common clock to be effected upon elapse of a fixed period of time (i.e., predetermined time) after said control circuit controls said switch circuit so as to turn on said bus connection for the advantage of obviating any drawbacks caused by a variation of frequency over a wide range (See Tsukamoto, col. 1, lines 42-57).

Referring to claim 4, Tsukamoto teaches output timing (i.e., T_e in Fig. 2) said data-transfer enable signal (i.e., frequency-switching end signal 19c in Fig. 2) output from said output circuit (i.e., clock frequency control 19 of Fig. 2) differs in dependence upon said access speeds of said devices (in fact, said output timing T_e is differing in dependence upon a new clock speed in α and β phases because the predetermined time is consisted of T_b and T_c, which are in time dependence upon said newly changed clock speed in α and β phases in Fig. 2).

Response to Arguments

9. Applicant's arguments with respect to claims 1-4 and 6 have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicant's arguments with respect to the amended claims 1-6, the Examiner brought Kelley and Tsukamoto references in the rejection for the limitations which are not provided by Nakajima and all of the other art cited.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hirai [US 6,255,882 B1] discloses method and system of switching clock signal.

Nakamura [JP 405094226 A] discloses clock switching system.

11. The Examiner considers Nakamura [JP 405094226 A] reference as a pertinent reference to applicant's disclosure in the instant Office Action, and it is referred to the original copy of foreign reference in foreign language (i.e., Japanese). The Examiner attaches a machine translated copy of the reference for the convenience of the Applicant. However, the Examiner cautions the Applicant that the Office is not responsible for any erroneous interpretation resulting from inaccuracies between the original foreign language reference and the machine translation of the reference, as the machine translation may not reflect the original precisely.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

cel/

Glenn A. Auve
Primary Patent Examiner
Technology Center 2100